The present invention has been developed in order to address the above drawbacks by providing a method of fabricating a semiconductor device, and by providing a semiconductor device obtained by the method. Although a description of the method and device of the present invention will now be provided with reference to various portions of the present application, reference to these portions is provided only for the Examiner's benefit, and is not intended to limit the scope of the claims to any specific embodiment.

As illustrated in, for example, Figures 5A-5C, the method of independent claims 8 and 11 recites mounting a plurality of semiconductor chips 20 on a plurality of leadframes 12, wherein the leadframes are arranged side by side and separate from each other. Grooves 60 are formed by cutting all of the leadframes 12 directly under the second main surface 20b of each of the semiconductor chips 20 in a direction orthogonal to the direction of elongation of the leadframes 12. The leadframes are then *cut between the semiconductor chips so as to form a plurality of semiconductor devices having a first external terminal row 14X of cut leadframes 14a, a second external terminal row 14Y formed of the cut leadframes 14b* and facing the first external terminal row 14X so as to sandwich one of the grooves 60 therebetween. One of the semiconductor chips 20 is mounted ***on*** the first external terminal row 14X *and* the second external terminal row 14Y.

The Minamio reference teaches a method of fabricating a semiconductor device including mounting a semiconductor element 3 on a die pad 1, and connecting the semiconductor 3 to inner leads 4 at the sides of the semiconductor element 3 (see Figures 1B and 1C). In the outstanding Office Action, the Examiner asserted that each of the semiconductor chips 3 is "placed over" several of the linear leadframes. Furthermore, in responding to the Applicants' previous arguments in item 9 of the Office Action, the Examiner asserted that the die pad 1 of the Minamio reference is part of the leadframes. However, even assuming that the Examiner's interpretation is correct, it is submitted that the Minamio reference still does not teach or suggest the features recited in independent method claims 8 and 11.

In particular, the Minamio reference does not teach or suggest forming grooves by cutting all of the leadframes directly under the second main surface of each of the semiconductor chips in a direction orthogonal to the direction of elongation of the leadframes, and then cutting the

leadframes to form a plurality of semiconductor devices each having *first external terminal row formed of the cut leadframes,* a *second external terminal row formed of the cut leadframes* and facing the first external terminal row so as to sandwich one of the grooves therebetween. In other words, even if the Examiner's position that the die pad 1 of the Minamio reference is part of the leadframe, it is noted that the die pad 1 is ***not*** an external terminal, and the leadframes are ***not*** cut in a manner so as to form first and second external terminal rows arranged as recited in independent claims 8 and 11. Furthermore, although the Examiner noted that each of the semiconductor chips 3 is "placed over" several of the linear leadframes, the Minamio reference does not teach or suggest that one of the semiconductor chips is *mounted on* a first external terminal row and a second external terminal row. To the extent that the die pad 1 is part of the leadframe unit of the Minamio reference, the lead pad 1 clearly does not constitute first and second external terminal rows on which a semiconductor chip is mounted. Accordingly, it is respectfully submitted that the Minamio reference does not anticipate or even suggest the method recited in independent method claims 8 and 11.

Independent claim 14 is directed to a semiconductor device having a plurality of *first external terminals* 14a spaced apart from each other, and a plurality of *second external terminals* 14b spaced apart from each other. As illustrated in Figure 5C, the plurality of first external terminals 14a and the plurality of second external terminals 14b are arranged so as to be spaced apart and oppose each other across a gap 60. A semiconductor chip 20 is *mounted **on*** the plurality of first external terminals 14a and the plurality of second external terminals 14b so that the second main surface of the semiconductor chip 20 faces the plurality of first external terminal and the second external terminals.

As explained above with respect to independent claim 8 and 11, the Examiner asserted that the Minamio reference teaches semiconductor chips "placed over" several linear leadframes. Furthermore, in response to the Applicant's previous arguments that the semiconductor chip 3 of the Minamio reference is actually mounted on a die pad 1 rather than external terminals, the Examiner asserted that the die pad 1 is part of a leadframe unit. However, assuming the Examiner's interpretation is correct, it is submitted that the Minamio reference still does not

disclose or suggest first external terminals spaced apart from each other, second external terminals spaced apart from each other and spaced apart from and opposing the first external terminals, and a semiconductor chip *mounted on* the first external terminals and the second external terminals. As explained above, the die pad 1 does not constitute an external terminal, and a semiconductor chip "placed over" linear leadframes does not constitute having the semiconductor chip *mounted **on*** the leadframes (even assuming the linear leadframes are external terminals). Accordingly, it is respectfully submitted that the Minamio reference does not anticipate or even suggest the semiconductor device as recited in independent claim 14.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. However, if the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact the Applicant's undersigned representative.

Respectfully submitted,

Hidenori HASEGAWA

By:_____

W. Douglas Hahm
Registration No. 44,142
Attorney for Applicant

WDH/ck
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
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